Faculty of Information and Communication Engineering

M.E. VLSI Design

(R 2017) Semester – I
VL7111 VLSI Design Laboratory I

(Requirements for a batch of 25 students)

Sl. No.	Description of Equipment	Quantity required (R)	Quantity available (A)	Deficiency (R - A)
1.	Xilinx / Equivalent EDA tool	15		
2.	FPGA - Altera / Sparton boards	15		
3.	Logic Analyzer	7		
4.	DSO	7		
5.	Interface Board - ADC	2		
6.	DAC	2		
7.	Motor Control	2		
8.	SPICE Software	15		

Faculty of Information and Communication Engineering

M.E. VLSI Design

(R 2017) Semester – II

VL7211 VLSI Design Laboratory II

(Requirements for a batch of 25 students)

Sl. No.	Description of Equipment	Quantity required (R)	Quantity available (A)	Deficiency (R - A)
1.	CADENCE / TANNER / Mentor Graphics / Synopses	15		