TECHNICAL (ONLINE) SESSIONS ON CUSTOM ANALOG DESIGN FLOW USING CADENCE VIRTUOSO BY CHIPIN

We would like to inform that ChipIN Centre, CDAC is conducting an online technical training session on Custom Analog Design Flow using Cadence Virtuoso for all C2S participating institutions.

Day-1	05/April/2024 & 2:30pm to 5:00pm	Schematic entry and Spectre Analysis (will be covered by ChipIN Team)
Day-2	16/April/2024 & 2:30pm to 5:00pm	Custom Layout Design, Verification and Post-Layout Analysis (will be covered by ChipIN Team)
Day-3	19/April/2024 & 2:30pm to 5:00pm	Virtuoso Initial Setup, Schematic Design, Pre-Layout Simulation Setup Using ADE Explorer and Assembler, Running Simulations, etc. (will be covered by Cadence Team)
Day-4	22/April/2024 & 2:30pm to 5:00pm	Dummy Transistors, Shielding, Latch-Up, Guard Ring, PCell Design for MOS & Passive Devices, Layout XL Overview, Post-Layout Simulation, etc. (will be covered by Cadence Team)

MEETING DETAILS

Join from a video conferencing system or application

Dial	: chipin@cdacb.webex.com
Meeting link	: https://cdacb.webex.com/meet/chipin
Meeting number	: 2511 322 7261

The Cadence tools used in this session are available to College of Engineering Guindy Campus, Anna University, free of cost. For installation of Cadence tools and if there is any difficulty in joining the above mentioned online training session, Chief Investigator and Co- Chief Investigators of C2S project, Centre for Wireless System Design can be reached for assistance.

Please find below the mail ids for assistance

- j_dhurgadevi@annauniv.edu
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Technical (Online) Sessions on Custom Analog Design Flow
(April 05th, 16th, 19th and 22nd, 2024)

Time	Topics	Prerequisites	Cadence Tools used
Day-1 (05-04-2024) – will be covered by ChipIN Team			
2:30 pm to 4:30pm	• Schematic Entry, Symbol Creation and Testbench Creation. • Spectre Analysis: DC, AC, Trans-w noise (Gain, Spectrum, Slew Rate, Power (DC & Avg), Input Offset, CMRR, PSRR, Stability, Noise	1. Virtuoso version 6.1.7-64b 2. Spectre version 18.1.0 64bit 3. Primitive Library (as listed in Virtuoso) – ts018_scl_prim 4. Spice Library - ts18sl_scl.lib	Virtuoso & Calibre
4:30pm to 5:00pm	Q & A Session	--	--
Day-2 (16-04-2024) - will be covered by ChipIN Team			
2:30 pm to 4:30pm	• Custom Layout Design: MIM cap layout, Resistor layout,Opamp layout. • Physical Verification: DRC, ARC, LVS, PEX, CDF edit, Spectre view. • Post-Layout Analysis: High Performance Simulation, Multi-Technology Simulation, PVT, Monte Carlo.	1. Virtuoso version 6.1.7-64b 2. Calibre v2017.4_35.25 Calibre Utility Library v0-8_2-2017-1 Litho Libraries v2017.4_35.25 3. spectre version 18.1.0 64bit 4. Primitive Library (as listed in Virtuoso) – ts018_scl_prim 5. Spice Library - ts18sl_scl.lib 6. DRC Doc - DR2_0018SL_SCL_Rev1.pdf 7. DRC Rule Set – DRC_BLOCK.header 8. ARC Rule Set – ANTENNA.header 9. LVS Rule Set – LVS.header 10. PEX Rule Set – RCX_4LM.header 11. Spice Library for Monte Carlo - ts18sl_scl_mat.lib	Virtuoso & Calibre
4:30pm to 5:00pm	Q & A Session	--	--

Time	Topics	Prerequisites	Cadence Tools used
Day-3 (19-04-2024) Front End – (will be covered by Cadence Team)			
2:30 pm to 4:30pm	• Virtuoso Initial Setup • Schematic Design • Pre-Layout Simulation Setup Using ADE Explorer and Assembler • Running Simulations - (DC, AC, Trans, Monte Carlo, Corner Analysis) • Multi-Technology Simulations • Visualization and Analysis of Results using ViVA	Tool Installation is must	Virtuoso
4:30pm to 5:00pm	Q & A Session		
Day-4 (22-04-2024) Back End – (will be covered by Cadence Team)			
2:30 pm to 4:30pm	• Dummy Transistors • Shielding, Latch-Up • Guard Ring • PCell Design for MOS & Passive Devices • Layout XL Overview • Post-Layout Simulation Setup Using ADE Explorer and Assembler • Accessing support.cadence.com Web Page	Tool Installation is must	Virtuoso
4:30pm to 5:00pm	Q & A Session		

Note: Please ensure that you meet the above-mentioned prerequisites before attending the online sessions.